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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/922,950 | 08/07/2001 | Manabu Koga | AMA.040 | 9509 |

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| EXAMINER | |
|---|---|
| DOAN, DUC T | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2188 | |

DATE MAILED: 12/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/922,950 | KOGA, MANABU | |
| | Examiner | Art Unit | |
| | Duc T. Doan | 2188 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/28/04 11/14/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Status of Claims*

1. Claims 1-12 are in the application.

Claims 1-12 are rejected.

### *Specification*

2. The disclosure is objected to because of the following informalities:

Column 9 line 19 cites the command RAM 12 is arraigned in the address range from 00000000h to 01000000h which overlaps with those of external memory 15.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claim 1,3 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's admitted prior art (APA).

As in claim 1, APA discloses a microcomputer comprising: a cache (Fig 1:#47), a central processing unit (Fig 1:# 42), said cache and said central processing unit both being fabricated in one chip (Fig 1:#41); and a memory (Fig 1:#51) storing commands to be executed by said central processing unit, said memory storing interruption handling routine therein. In column 2 lines 1-5, APA describes if interruption-handling routine were not in cache, it would be retrieved from memory 51.

As in claim 3, a memory component comprised of a random access memory (RAM) is inherent in the APA, since the external memory is accessed when cache miss occurs, and this requires random access.

***Claim Rejections - 35 USC § 103***

4. Claim 2,4,5,7-12, rejected under 35 U.S.C. 103(a) as being unpatentable over APA in view of Yaegawa et al (US 6598137).

As in claim 2, APA describes a computer with a memory capable of storing a program, interrupt handling routine, (column 2 lines 1-5). However, APA does not teach switching memory maps. Yaegawa (column 3 lines 59-67, column 4 lines 1-5) teaches a computer using a control section to move program data from a boot ROM into a non-volatile memory. Yaegawa (Fig 3) describes distinct address spaces for different memory spaces such as bootROM, non-volatile memory, and RAM memory (Fig 4). The control section thus readily switches memory maps to direct the computer to proper location of source and destination

addresses. Yaegawa teaches that the program can be transferred from non-volatile address space to RAM address space (column 4 lines 27-49). Yaegawa further teaches program residing in RAM is executed faster and can operate concurrently with another program being run out of non-volatile memory. (column 4 lines 51-61). Executing a program out of RAM is efficient due to the inherently fast access time of RAM. After program is transferred out of slow access devices (bootROM) into RAM memory, the bootROM does not need to be accessed anymore (column 4 line 11). It would have been obvious to one of ordinary skill in the art at the time of invention to include the RAM structure of Yaegawa in the APA and writing the program into the RAM in view of Yaegawa's teaching, thereby increasing the access speed of the program.

As in claim 4, APA describes a prior art computer system with central processing unit (Fig 1:#42); bus controller (Fig 1:#44); command cache (Fig 1:#47) and buses to interconnect the above elements . Bus 1 (Fig 1:#43); bus 2 (Fig 1:#45); bus 3 (Fig 1:#46); bus 5 (Fig 1:#48); bus 7 (Fig 1:#50). APA does not describe the command memory (Fig 2:#12) and the two buses bus 4 (Fig 2:#4); bus 6 (Fig 2:#6) which allow the command memory to communicate with CPU and external memory;. Yaegawa describes a computer with the command memory (Fig 2:#3); and buses to connect the command memory to CPU (Fig 2:#2) and to external bootROM (column 2:#5). Yaegawa teaches the command memory (Fig 2:#3) capable of storing interrupt handling program (column 4 line 30-42). It would have been obvious to one of ordinary skill in the art at the time of invention to add the command memory RAM structure of Yaegawa in the APA

and to store interrupt handling program in the RAM in view of Yaegawa's teaching, thereby increasing the speed of accessing the program.

As in claim 5, APA discloses a memory controller (Fig 1:#49); bus controller (Fig 1:#44); a fifth bus (Fig 1:#48) connecting memory controller and bus controller; a seventh bus (Fig 1:#50) connecting memory controller and external memory. APA does not disclose the sixth bus connecting memory controller to command memory. Yaegawa teaches a computer comprises of a RAM memory capable of storing command data (Fig 2:#3); and communication paths (bus 4 and bus 6) connecting the RAM memory to CPU and external bootROM. Yaegawa teaches a control section capable of transferring data from bootROM to RAM memory (column 4 lines 36-41). It would have been obvious to one of ordinary skill in the art at the time of invention to include the RAM structure and the control section of Yaegawa in the APA connecting to CPU and external memory in view of Yaegawa's teaching to provide direct communication paths for CPU, RAM and external memory.

As in claim 6, it describes the inherent features of a cache operation, cache hit and miss sequences. If command data exists in cache (cache hit), central processing unit reads and executes command data from cache. If command data does not exist in cache (cache miss), central processing unit reads and executes command data from external memory (Fig 1:#15).

Claim 7 is rejected using the same rational as for the rejection of claim 4. Notice Yaegawa further cites a prior art teaching CPU would transfer to execute

program in RAM whereas interrupt occurs. (column 3 lines 65-67 and column 4 line 32-34).

As for claim 8,9,10, and 11 APA does not disclose the control means for address mapping. Yaegawa teaches a control section translates addresses among different memory address spaces. Inherently control section must have a set of registers to keep information about memory address spaces. The location of control section is not restricted (column 4 line 36-39). Yaegawa further teaches the control section can be operated concurrently with other action of the central processing unit (column 4 line 54 –59). It would have been obvious to one of ordinary skill in the art at the time of invention to include the control section of Yaegawa in the APA to control the address space switching in view of Yaegawa's teaching to allowing programs to be executed either from command RAM or from external memory.

Claim 12 is rejected using the same rational as for the rejection of claim 3.

### *Conclusion*

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 6651152 Ueki et al. 11/18/2003. Microcomputer having build-in nonvolatile memory for simultaneous use as a program area and a data area. Ueki describes a memory switching device allowing data to be uploaded from external device. It is capable of operating concurrently with the central processor unit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mano Padmanabhan 12/12/04

DD

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER